

PATENT APPLICATION  
Do. No. 1138-071

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Dah Wen Tsang; John W. Mosier II, deceased;  
Douglas A. Pike, Jr., and Theodore O. Meyer

Serial No.: 09/144,579

Examiner: S. Loke

Filed: August 31, 1998

Group Art Unit: 2811

For: SELF ALIGNED VERTICAL POWER MOSFET  
WITH ENHANCED BASE REGION

14/F+  
attach

FJONES

3-15-02

BOX RCE  
Assistant Commissioner for Patents  
Washington, D.C. 20231

FAX COPY RECEIVED

DEC 4 - 2001

TECHNOLOGY CENTER 2800

## AMENDMENT

Responsive to the Final Office Action dated August 6, 2001 for which a one month extension is requested on the accompanying Request for Continued Examination (RCE) Transmittal, please amend the application as follows.

In the Specification:

On page 12, before line 4, insert as follows:

-- U.S. Pat. No. 4,895,810, incorporated by reference herein, teaches exemplary metal processes to reduce resistance across a surface of the gate polysilicon between the two sidewall spacers. Referencing FIGS. 6B (FIG. 19 of U.S. Pat. No. 4,895,810), a metal layer of substantial electrical conductivity, preferably 500 to 1,000 angstroms of tungsten, is deposited by selective CVD deposition to form ohmic contacts 275, 276 in silicon trench 263 and on the polysilicon layer 232. This means of tungsten deposition preferentially metallizes the exposed silicon (new layer 275) and polysilicon (new layer 276) surface but not the oxide sidewalls 262a. Alternatively, contacts 275, 276 can be made by selective silicide formation.